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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/623,646	03/02/2001	Peter Kennington	46387/247138	6290

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MENDELSOHN AND ASSOCIATES PC
1515 MARKET STREET
SUITE 715
PHILADELPHIA, PA 19102

EXAMINER	
LUGO, DAVID B	
ART UNIT	PAPER NUMBER
2637	

DATE MAILED: 02/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/623,646	KENINGTON, PETER	
	Examiner	Art Unit	
	David B. Lugo	2637	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *19-33 and 37-61* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *19-33,37 and 38* is/are allowed.

6)☒ Claim(s) *41-49,54,55 and 59* is/are rejected.

7)☒ Claim(s) *39,40,50-53,56-58,60 and 61* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. In the amendment to the specification, filed 9/7/04, changes indicated to be made to the paragraph starting at page 2, line 2 can not been entered as the page number indicated is incorrect. Please submit an additional amendment indicating the changes to be made at the correct portion of the specification (paragraph beginning at page 1, line 2).

Claim Objections

2. Claims 39-40 are objected to because of the following informalities:

a. Claim 39, line 10, "the direct current signal" should be --a direct current signal--.

b. Claim 39, line 10, "the second squared signal path" should be --a second squared signal path--.

c. Claim 39, lines 11-12, "the fifth order signal" should be --a fifth order signal--.

d. Claim 40 is objected to based on its dependency from claim 39.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 41-44 and 46 are rejected under 35 U.S.C. 102(b) as being anticipated by Nojima et al. U.S. Patent 4,329,655.

5. Regarding claim 41, Nojima et al. disclose a predistorter for linearizing an amplifier in Fig. 5 comprising a first set of circuitry (5a) for generating a first high-order signal based on an input signal, which is used to generate a predistorted input signal for application to the amplifier, and the order of the first high-order signal is equal to 5.

6. Regarding claim 42, the predistorter further comprises a second set of circuitry (5) for generating a second high-order signal based on the input signal, where the first and second high-order signals are used to generate the predistorter signal and the order of the second high-order signal is equal to 3.

7. Regarding claim 43, both the first and second high-order signals are odd-order signals.

8. Regarding claim 44, the first high-order signal is a fifth-order signal and the second high-order signal is a third-order signal.

9. Regarding claim 46, the first and second sets of circuitry are independently controlled via control signals sent thereto from distortion control circuit 13.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 45, 48, 54, 55 and 59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nojima et al. in view of Seidel U.S. Patent 3,732,502.

12. Regarding claim 45, Nojima et al. teach a predistorter circuit as described above, but do not expressly disclose a third set of circuitry adapted to generate a seventh-order signal.

13. Seidel discloses a predistorter circuit that can compensate the n-th order of an amplifier (see Fig. 1).

14. It would have been obvious to one of ordinary skill in the art to use the teaching of Seidel to generate a seventh-order signal in the predistorter circuit of Nojima et al. in order to linearize the amplifier up to the seventh order.

15. Regarding claim 48, Nojima et al. disclose a predistorter as described above, and further disclose that the second high-order signal is a third-order signal, but do not disclose what the second set of circuitry for generating the third-order circuit comprises.

16. Seidel discloses a third-order signal generator in Fig. 5, where a first combiner 57 is adapted to combine first and second versions of the input signal to generate a second-order signal, and a second combiner 58 is adapted to combine a third version of the input signal with the second-order signal to generate the third-order signal.

17. It would have been obvious to one of ordinary skill in the art to use the third-order signal generator of Seidel in the system of Nojima et al. in order to provide the desired third-order signal.

18. Regarding claim 54, Nojima et al. disclose that the first high-order signal is a fifth-order signal (col. 8, lines 54-55).

19. Regarding claim 55, Nojima et al. do not disclose that the first set of circuitry comprises a third combiner to combine a version of the second-order signal with a version of the third-order signal to generate the fifth-order signal.

20. Seidel discloses that a fourth order compensating network may be used to compensate an amplifier to the fifth order (col. 6, lines 54-59), where the fourth order compensating network,

shown in Fig. 6, includes a combination of a second-order signal generated via block 65 with a third-order signal generated via block 66.

21. It would have been obvious to one of ordinary skill in the art to generate a fifth-order signal as taught by Seidel in the system of Nojima et al. as a matter of design choice, as multiple methods may be used to generate a fifth-order signal.

22. Regarding claim 59, Nojima et al. do not disclose that the first set of circuitry comprises a third combiner to combine a third version of the input signal with a third-order signal to generate a fourth-order signal, and a fourth combiner to combine a fourth version of the input signal with the fourth-order signal to generate the fifth-order signal.

23. Seidel discloses that a fourth order compensating network may be used to compensate an amplifier to the fifth order (col. 6, lines 54-59), where the fourth order compensating network, shown in Fig. 6, includes a combination of the input signal with a third-order signal generated via block 66 to generate a fourth order-signal, where the fourth-order signal is further combined with the input signal to generate a fifth-order signal (col. 6, lines 57-59).

24. It would have been obvious to one of ordinary skill in the art to generate a fifth-order signal as taught by Seidel in the system of Nojima et al. as a matter of design choice, as multiple methods may be used to generate a fifth-order signal.

25. Claim 47 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nojima et al. in view of Wilson U.S. Patent 5,812,294.

26. Regarding claim 47, Nojima et al. disclose a predistorter circuit as described above, further comprising a variable phase-shift block 6 and a variable attenuator block 7 adapted to apply a selected phase shift and a selected attenuator level, respectively, to each of the first and

second high-order signals, and a summation node for combining the phase-shifted, attenuated, first and second high-order signals to form a polynomial predistortion signal.

27. Nojima et al. do not expressly disclose an amplifier for amplifying the polynomial predistortion signal, and a second summation node for combining the amplified, polynomial predistortion signal with the input signal to generate the predistorted input signal.

28. Wilson discloses a predistorter in Fig. 2 comprising an amplifier (gain G) connected to an odd-order nonlinearity circuit for providing a gain to a combined third-order and fifth order predistortion signal, where the amplified signal is combined with the input signal to generate the predistorted input signal.

29. It would have been obvious to one of ordinary skill in the art to provide a gain to the predistortion signal before combining the signal with the input, as taught by Wilson, in the predistorter of Nojima et al. in order to adjust the gain of the combined signal to the appropriate level.

30. Claim 49 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nojima et al. in view of Seidel and Alinikula U.S. Patent 5,786,728.

31. Regarding claim 49, Nojima et al. and Seidel disclose a predistorter as described above, but do not disclose that the first and second combiners are mixers.

32. However, using mixers as combiners in a predistortion circuit is well known in the art. For example, Alinikula teaches the use of mixers (15, 16) for combining signals. The use of mixers for the combiners are deemed a design consideration that fails to patentably distinguish over the prior art, and it would have been obvious to one of ordinary skill in the art to use mixers as a matter of design choice.

Allowable Subject Matter

33. Claims 19-31, 32, 33, 37 and 38 are allowed.

34. Claims 39 and 40 would be allowable if rewritten or amended to overcome the objections set forth in this Office action.

35. Claims 50-53, 56-58, 60 and 61 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

36. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David B. Lugo whose telephone number is 571-272-3043. The examiner can normally be reached on M-F; 9:30-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on 571-272-2988. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

David B. Lugo
2/1/05

KHAI TRAN
PRIMARY EXAMINER